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Multidisciplinary Block Program

ADVANCED SUPERCONDUCTOR DIGITAL ELECTRONICS

DoD's University Research Initiative
Multi-Agency Topic
"Low-Temperature Superconductor Digital Electronics"

(AFOSR Grant # F49620-95-1-0415)

Final Report

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December 1998

Contents

Executive Summary

The 5-year multidisciplinary program *Advanced Superconductor Digital Circuits* within the framework of DoD's University Research Initiative was started at SUNY Stony Brook in September 1992. (During the first 3-year period it was supported via the AFOSR Grant #F49620-92-J-0508, and after that date via this grant.)

The main focus of the program was the development of ultrafast superconductor devices and circuits based on the storage, transfer, and processing of digital bits encoded by single quanta of magnetic flux. This approach offers several key advantages over other possible digital technologies, including a very high operation speed and extremely low power consumption.

During the first 3-year period of the program, substantial progress in the development of these Rapid Single-Quantum-Flux (RSFQ) devices and circuits was achieved. Simultaneously, important improvements were made in design, fabrication, and testing capabilities of our Stony Brook group.

This background allowed us to achieve important goals during the second stage of the program. Most importantly, we have demonstrated several RSFQ circuits with integration scale as high as allowed by the existing fabrication technology (a few thousand Josephson junctions). We have also developed a new fabrication technology featuring non-hysteretic submicron Josephson junctions, and used it to reach an unparalleled speed (770 GHz) in simple RSFQ circuits. Important contributions were also made to the theory of the Josephson effect in ballistic and diffusive point contacts which apparently determine the observed properties of submicron junctions with very high critical current density.

Also, a dozen undergraduate and graduate students have received substantial training in various aspects of superconductor electronics.

We believe that the original goals of the URI program have been met, and in some areas, surpassed. This program has resulted in considerable progress in RSFQ technology which continues to be developed by several groups (including our Stony Brook group) within the framework of other R&D programs.

1. Introduction: RSFQ Technology and Stony Brook Program

The main focus of our program was the development of ultrafast superconductor digital devices and circuits of the Rapid Single-Flux-Quantum family (for reviews, see Refs. 1, 2). In this family of devices, the binary information is stored in superconducting loops in the form of the number N of trapped quanta of magnetic flux. The loops include one or several overdamped Josephson junctions which allow the state of the loop to be changed (i.e. a single flux quantum injected or extracted) during a very short time interval. This interval is ultimately limited only by superconductor energy gap, and for low-temperature superconductors (e.g., Nb) may be below one picosecond.

A change in the number of flux quanta in the loop results in the formation a picosecond "Single-Flux-Quantum" (SFQ) pulse of voltage. In circuits of the RSFQ family, these picosecond pulses are used for the transfer and processing of digital bits. The logic gates ("elementary cells") of this family have natural intrinsic memory and may be clocked by SFQ pulses [1, 2]. The advantages of this approach include:

- a natural reset of logic gates on the picosecond time scale;
- possibility of data transfer at a speed approaching that of light;
- flexible combination of synchronous and asynchronous timing;
- dc power supply.

Theoretical analysis shows [1] that these features allow the implementation of complex RSFQ circuits with extremely high clock frequencies, potentially in excess of 100 GHz, i.e. at least two orders of magnitude higher than that of the fastest semiconductor VLSI circuits. Other advantages of the RSFQ approach include very small power consumption (fundamentally limited only by thermal fluctuations, at helium temperatures to ~10^{-18} joule per bit) and relatively simple fabrication technology.

The main problem with low-T_c RSFQ technology is the necessity of helium cooling which is very inconvenient for many potential users. A possible solution to this problem is reaching a decisive leading edge in performance (first of all, in speed) which would outweigh the burdens of refrigeration.

In the initial proposal of our multidisciplinary program, the basic goal was formulated as follows: "*to pave the way to practical superconductor circuits and systems based on* [RSFQ] *devices*". What follows is a list of the main results in major directions of our work.

2. Main Results

A. Fundamentals

A.1. Quantum Fluctuations at RSFQ Switching [3]

Earlier in the program we studied fluctuation-induced smearing of the threshold of switching of a typical component of RSFQ circuits, a balanced Josephson junction comparator, by an SFQ pulse. The measured smearing has been found to be in a nice agreement with the results of theory based on thermally-induced fluctuations. During the report period, we extended these theoretical and experimental studies to the case of finite time interval between the input pulses, and to junctions with higher critical current density (j_c ~ 5 kA/cm^2), fabricated at Stony Brook. In these junctions, we have succeeded in obtaining strong evidence of quantum fluctuations with almost negligible temperature dependence in the interval from 2.2 to 4.2 K. The data have turned out to be in good quantitative agreement with quantum-statistical theory based on the Hamiltonian suggested by Caldeira and Leggett. These results are of primary importance for the prospective submicron versions of the RSFQ technology which will require even higher values of j_C and as a result will lead to even larger quantum fluctuations, thus squeezing the window of parameters available for reliable operation of RSFQ circuits.

A.2. Pulse Jitter and Timing Errors in RSFQ Circuits [4, 5]

We have carried out measurements of bit error rate (BER) of RSFQ XOR gates with various nominal dc power supply voltages (from 0.1 V to 1.0 mV), operating at speed up to 25 GHz. (For these gates, implemented using HYPRES' standard, 3.5-μm, 1-kA/cm^2, Nb-trilayer process, this speed is close to maximum.) A special on-chip RSFQ test circuit has allowed accurate measurements of BER in the range from 10^{-9} to 10^{-13} to be carried out. As a result of these experiments, a new type of thermal-fluctuation-induced digital errors in RSFQ circuits has been identified. These "timing" errors arise at high speed due to time jitter of data and clock pules. We have developed a simple theory of these errors which allows a fair description of the experimental data, and have applied it to both basic RSFQ blocks and such complex circuits as bit-parallel, pipelined adders. The theory shows that in some cases the timing errors may be an important factor limiting speed performance of RSFQ circuitry.

A.3. Ultra-low-power RSFQ circuits [4, 6]

We have explored the opportunity of a further reduction of power consumption of RSFQ circuits. Though a radical solution (which would permit the fundamental limit of dissipation to be reached) would require the development of a completely new library of RSFQ cells, we have shown that this limit may be approached by merely reducing the dc supply voltage of the conventional RSFQ cells. Our analysis has shown that for the current (3.5-μm, 1 kA/cm^2) generation of niobium-trilayer technology, transfer from the traditional, 2.6-mV supply to 0.6-mV supply (with the corresponding 4-fold decrease in power dissipation) may involve only a modest 5% reduction of parameter margins.

Experimentally, we have demonstrated RSFQ gates operating at 25 GHz with BER below 10^{-13} at the standard temperature (4.2 K). For a dc supply voltage of 0.1 Volt the static power dissipation in the gate was as low as 23 nanowatts, lower than the unavoidable dynamic dissipation (43 nanowatts).

B. Logistics

B.1. Multi-Chip Modules [7]

The development of prospective RSFQ systems depends on the availability of multi-chip modules with multi-GHz communication bandwidth. We have developed a simple cryogenic multi-chip module using flip-chip bonding with low-temperature solder bumps. The bonding has proven to give good dc contacts for all 36 contact pads of our standard 5x5-mm^2 chips, without shorts between them.

B.2. New Testing Methods [8]

We have developed several new methods of testing the physical parameters of RSFQ components and circuits. One of these methods allows the study of parameter spreads, thermal fluctuations, and flux trapping in sizable RSFQ circuits using very few contact pads. Extraction of the parameters of interest has been completely automated. Testing data has been made available to personnel at HYPRES, Inc., who are responsible for circuit fabrication.

B.3. PSCAN'96 and JULIA [9, 10]

Through all the years of our project, incremental improvements have been made to our basic software tool, PSCAN (Personal Superconductor Circuit ANalyzer) which was first introduced in 1991. In 1996, a number of gradually accumulated changes of PSCAN were merged into a new version of the simulator, called PSCAN'96. Unfortunately, this work has never been fully completed because of creative difference of opinion between its numerous participants. Instead of this, a completely new program (retaining the basic ideas of PSCAN) called JULIA has been written. We expect that after a debugging period this program will become the main RSFQ simulation tool in our laboratory and possibly in other groups

B.4. Extraction of 3D Inductances [11]

We have started to work on the development of a program which could extract mutual inductance matrices of 3D superconductor circuits, which should in future replace our current 2D extractor L-METER. This replacement will be especially important for high-T_C RSFQ circuits with their large London penetration depth, and high-j_C circuits with their submicron feature sizes. We have completed the first version of this program, a relatively simple computer code for single-layer circuits. Even at this stage, the program is quite useful for the analysis of some high-T_c and high-j_c circuit components.

C. Submicron Josephson Junctions: Technology and Physics

C.1. Submicron Nb-Trilayer Technology [12, 13]

We have developed a deep-submicron version of the planarized, Nb-trilayer fabrication technology, using electron beam lithography for Josephson junction definition. We have been able to demonstrate single Josephson junctions with effective area down to 0.006 μm^2 and critical current density beyond 300 kA/cm^2. These junctions exhibit non-hysteretic I-V curves with very respectable I_cR_N product of the order of 2 mV. Their *I-V* curves, however, differ substantially from those predicted by existing theories of the Josephson effect in tunnel junctions. (Such deviations have been reported earlier by other authors for lower values of j_C)

C.2. Ultra-high-frequency RSFQ Circuits [14, 15]

Using the developed submicron technology, we have demonstrated simple RSFQ devices (digital frequency dividers) which can operate at record speed. Two device versions were successfully tested. A divider with externally-shunted junctions with j_c = 50 kA/cm^2 (junction area A = 0.25 μm^2) can operate up to 750 GHz, while with a device with self-shunted junctions with j_c as high as 250 kA/cm^2 ($A \approx 0.1$ μm^2) we have reached 770 GHz. To our knowledge, these are the fastest digital circuits yet demonstrated. Another important feature of these devices is their extremely low power dissipation, of the order of 1 microwatt, the number to be compared with approximately 1 watt for the fastest (~50 GHz) semiconductor devices of comparable complexity. Maybe even more importantly, the demonstration of the first RSFQ devices with submicron, self-shunted Josephson junctions opens the way toward VLSI superconductor circuits with device density approaching 1 million gates per cm^2, quite comparable with that of the modern CMOS circuits.

C.3. Josephson Effect in Mesoscopic Point Contacts [16-20]

Earlier in our program, the first microscopic theory of the ac Josephson effect in ballistic point contacts was developed. The theory expresses transport characteristics of such junctions in terms of cycles of multiple Andreev reflections (MAR). During the report period, this theory was extended from single-mode to multi-mode junctions with arbitrary electron transmission statistics. This allowed us for the first time to calculate current-voltage characteristics of regular SNS junctions with diffusive electron transport in the N-region. The calculated characteristics are strikingly similar to experimental *dc I-V* curves of our submicron Josephson junctions with the critical current density of the order of higher than 100 kA/cm^2. This result allows us to hope that we are close to quantitative understanding of the transport properties of such junctions.

The MAR theory was also extended to fluctuation properties of such contacts. Surprisingly, extremely large current fluctuations in such systems, presumably induced by the Josephson supercurrent itself, have been found. If experimentally confirmed, this effect will be important for all Josephson junctions with highly transparent barriers,

including high-j_C junctions necessary for the development of submicron RSFQ circuits. Other applications of the theory were also studied, including smearing of the subgap current singularities by pair-breaking effects in the superconducting electrodes, and the structure of these singularities in constrictions between the composite superconducting-normal electrodes with the proximity-induced gap in the normal layer.

D. RSFQ Devices, Circuits, and Systems

D.1. Delay-Insensitive RSFQ Circuits [21-23]

In collaboration with researchers from Intel and University of Texas at Austin we have explored the opportunity of replacing the traditional RSFQ logic circuits (with explicit timing) by asynchronous ("delay-insensitive") circuits using dual-rail presentation of digital bits. A complete logic family based on this principle has been suggested, and several simple circuit primitives implemented and tested experimentally. Moreover, two delay-insensitive versions of the first sizable RSFQ circuit (parallel integer adder) have been developed and analyzed.

The results indicate that the new approach may offer certain advantages over the traditional circuits. One of these advantages is the opportunity to virtually exclude static power consumption in RSFQ circuits. Moreover, functional circuits using the delay-insensitive logic may have higher throughput than traditional RSFQ circuits using explicit timing. However, the former approach requires more complex circuits (the Josephson junction count may grow by a factor of two or so.) In this context, adequate applications for the asynchronous RSFQ circuits still have to be found.

D.2. A/D Converters [24-28]

Our first substantial achievement in the field of stand-alone RSFQ systems was the design and successful testing (in March 1996) of the first flux-counting oversampling analog-to-digital converter. The prototype ADC included 1,778 Josephson junctions incorporated in 117 gates and auxiliary circuits. It was laid out on a standard 5x5-mm^2 chip and dissipates as little as 0.5 milliwatt of power. The system has proved to be completely operational at sampling frequencies up to 11 GHz.

Later in the project, several other versions of the converter were tested. Finally, we have joined forces with HYPRES, Inc., and jointly designed the first ADC which was completely tested both on low and high frequencies. Though the performance of this device (12.0 effective bits at 10 MHz and 8.8 effective bits at 50 MHz) is slightly worse than that of the best semiconductor ADCs, we see several ready modifications which should boost the performance to, e.g., 14 effective bits at 60 MHz, i.e. well beyond the reach of traditional A/D conversion methods, even if the current rudimentary technology is used.

D.3. Digital SQUIDs [29, 30]

Most blocks of the A/D converter, notably the digital decimation filter, may be used to design a digital SQUID with a very high slew rate (~10^{10} Φ_0/s), which could be used in unshielded environments (e.g. for biomagnetic measurements and non-destructive evaluation). Presently, such a SQUID (including its interface with room-temperature electronics) has been designed and apparently debugged. Unfortunately, none of the chip copies received from fabrication was fully functional, presumably because of fabrication problems.

D.4. D/A Converters [31-33]

We have designed a 19-bit prototype of an RSFQ D/A converter. Such converters may combine an unprecedented accuracy of each voltage level (unlimited fundamentally at least up to ~10^{-15}) with short settling time (in prospect, below 50 ns). The digital part of the prototype has been successfully tested at low frequencies, though we still have a problem with its analog part (voltage multipliers). We believe we know the reasons for this problem, and are going to complete this work within the framework of another project (supported by NIST).

D.5. Digital Autocorrelators [6, 34, 35]

We have developed two versions of a single-bit digital autocorrelator with extremely wide signal bandwidth (a few GHz). A 16-channel version of the correlator has been completely tested at clock frequencies beyond 10 GHz. We have also suggested a new concept enabling the total number of channels to be increased dramatically (to 1,024 or so), making the device valuable for millimeter-wave radioastronomy and possibly other applications, without complex high-speed interchip connections.

D.6. Digital Packet Switching [36-40]

The unique speed of RSFQ circuits may be used in ultrafast self-routing, nonblocking switches for multiprocessor computers and communication systems. We have explored these opportunities theoretically, with a simultaneous analysis on the system, circuit, and device levels. The following 4 candidates for switching cores have been considered in detail:

- crossbar,
- Batcher-banyan,
- token ring,
- an original shared bus system with time-division multiplexing.

The analysis has shown that an RSFQ Batcher-banyan structure promises the lowest system complexity at a given performance. For example, a 128x128-channel switch using this architecture would use only 173,000 Josephson junctions and might fit on a single 1x1-cm^2 chip. If implemented using a 1.5-μm niobium-trilayer technology, such a switching core should provide unparalleled total throughput of 7.5 Tbps (60 Gbps per channel), while dissipating as little as 60 milliwatts of power.

Besides that, a new concept of credit-based flow control in self-routing switching networks has been suggested and tested. (This approach may also be useful for other RSFQ circuits.) A 2x2 switching node using this concept has been designed; the single-bit datapath part of the node has been implemented and successfully tested (so far, at low frequencies).

D.7. General-Purpose Computing [41]

In the beginning of our project we started to develop a simple microprocessor prototype which would be inferior to the modern semiconductor chips (because of low integration scale of the present-day superconductor technology), but would nevertheless demonstrate the unparalleled clock speed of RSFQ logic.

However, our effort was soon overshadowed by the petaflops initiative. The origin of the interest in petaflops-scale computing using RSFQ technology stems from the very low power consumption of RSFQ circuits which may be a decisive factor for very large computing systems. For example, our estimates show that a petaflops-scale RSFQ system would dissipate ~250 W at 4K (equivalent to ~100 kW at room temperature); the number to be compared with ~15 MW estimate for the best prospective CMOS systems of a similar performance.

In this context, our work on general-purpose computing has been transferred to (and is now continued within the framework of) another program supported by DARPA, NSA, and NASA. Our hopes are that this work will not only lead to the eventual development of high-end computing using superconductor electronics, but also will serve as a driver for other applications of RSFQ technology.

E. Education and Result Dissemination

In the course of the research work described above, more than a dozen undergraduate and graduate students (including A. Bardas, P. Bunyk, W. Chao, W. Chen, H. Imam, Y. Kameda, P. Litskevitch, S. Polonsky, A. Rylyakov, D. Schneider, P. Shevchenko, and D. Zinoviev), as well as a few postdocs and young visiting scientists from several institutions, have received substantial training in various aspects of superconductor physics and electronics.

Besides numerous original publications (see Sec. 3 below) and conference presentations by the members of our group, several reviews of the RSFQ technology [42-46] were written during the report period.

* * *

To summarize, we believe that the basic goals of the second 3-year stage of our program, as well as the URI program as a whole, have been successfully reached, and some of them have been surpassed. This program has fulfilled its mission, since it has resulted in considerable progress in RSFQ technology which continues to be developed within the framework of other R&D programs.

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